Sub D1 C1

1. (Three Times Amended) A semiconductor device, comprising:

a substrate; and

a multilayer interconnection structure formed on said substrate,

said multilayer interconnection structure including: at least first and second interlayer insulation films provided on said substrate; and a guard ring pattern embedded in each of said first and second interlayer insulation films, said guard ring pattern extending along a periphery of said substrate, said multilayer interconnection structure being planarized by using a CMP process,

wherein said guard ring pattern changes a direction thereof repeatedly and alternately in a plane parallel to said substrate,

said guard ring pattern including: a groove formed in each of said first and second interlayer insulation films, said groove changing a direction thereof repeatedly and alternatively in a plane parallel to said substrate, a conductive wall filling said groove in each of said first and second interlayer insulation films and extending from a bottom principal surface thereof to a top principal surface thereof; and a conductive pattern making a contact with a top part of said conductive wall and having a principal surface coincident to said top principal surface of said interlayer insulation film, said conductive wall changing a direction thereof repeatedly and alternately in one of a triangular wave pattern and a rectangular wave pattern in said plane in correspondence to said guard ring pattern,

said conductive wall in said first interlayer insulation film being offset with respect to said conductive wall in said second interlayer insulation film in a direction parallel to a principal surface of said substrate when viewed in a direction perpendicular to said principal surface of said substrate,

and wherein said interlayer insulation films comprise a first insulation film that supports said conductive wall laterally and a second insulation film that supports said conductive pattern laterally.

C2

7 (Amended) A semiconductor device as claimed in claim 1, further comprising an etching stopper layer interposed between said first insulation film and said second insulation film.